PATENT ABSTRACTS OF JAPAN

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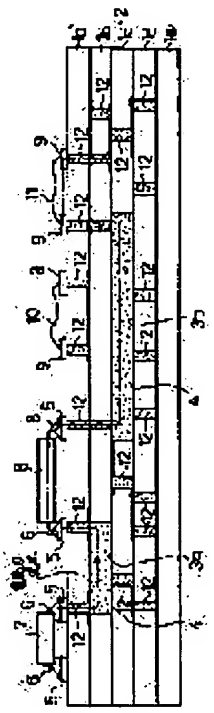
(21)Application number : 03-177010
(22)Date of filing : 17.07.1991

(71)Applicant : NIPPONDENSO CO LTD
(72)Inventor : NAGASAKA TAKASHI

(54) MULTILAYERED SUBSTRATE

(57)Abstract:
PURPOSE: To provide the title multilayered substrate capable of lessening the wiring resistance values.
CONSTITUTION: A hybrid IC is formed into the title multilayered substrate 2 laminating five alumina insulating layers 1a-1e. At this time, an inner layer wiring through-trench 3a is formed in the insulating layer 1b of the multilayered substrate 2 filled up with an inner layer wiring material 4. Likewise, another inner layer wiring through-trench 3b is formed in the insulating layer 1c of the multilayered substrate 2 filled up with the inner layer wiring material 4. These inner layer wiring through-trenches 3a, 3b are made to be a band shape.



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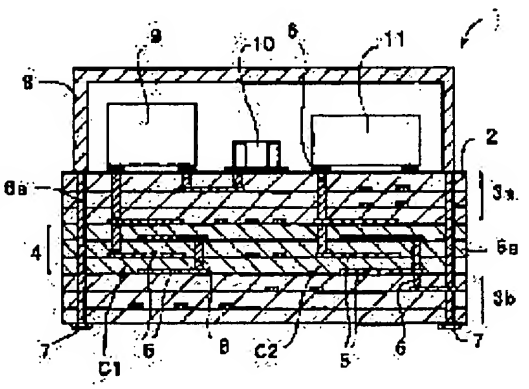
(21)Application number : 2000-385564
(22)Date of filing : 19.12.2000

(71)Applicant : MURATA MFG CO LTD
(72)Inventor : SUGIMOTO YASUTAKA
CHIKAGAWA OSAMU
MORI NAOYA

(54) COMPOSITE LAMINATED CERAMIC ELECTRONIC PART AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a composite laminated ceramic electronic part which is hardly deformed and separated from its interface with an operating material, can be baked at a low temperature, is suitable for radio waves of high frequency, and has a low dielectric loss.
SOLUTION: A composite laminated ceramic electronic part is a laminate composed of a high-permittivity dielectric layer which is formed of high- permittivity dielectric material that contains a main component represented by a composition formula, BaO-{(1-y)TiO2.yZrO2} (wherein, 3.5≤x ≤4.5, 0≤y≤0.2), and an auxiliary additive and has a relative permittivity εr of 20 or above. At least a low-permittivity layer which is formed of low-permittivity material of a composite composed of ceramic and glass composition and has a relative permittivity εr of 10 or below.



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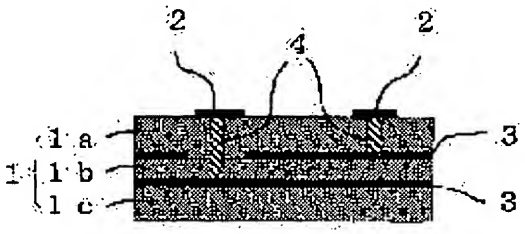
(22)Date of filing : 28.03.2001

(71)Applicant : KYOCERA CORP
(72)Inventor : SUZUKI SHINICHI
NAGAE KENICHI
NAKAO YOSHIHIRO

(54) MULTILAYER WIRING BOARD

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the increase in capacitance of a built-in capacitor due to simultaneous baking by adjusting the material composition of a high dielectric layer and low dielectric layer.
SOLUTION: In a multilayer wiring board in which a conductive wiring layer 2 is arranged on the surface of the inside of a ceramic insulating substrate 1 which is a laminate of a high dielectric layer 1b and low dielectric layers 1a and 1c, the layer 1b contains CaTiO3 and the amount of Ca in the layers 1a and 1c is set at 20% or more of the total amount of Ca in the layer 1b. By the way, both layers 1a and 1c are preferably made of sintered bodies obtained by adding an inorganic filler to an SiO2-BaO-CaO-Al2O3-B2O3 based glass and sintering the resulting bodies.



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(51)Int.Cl. H05K 3/46
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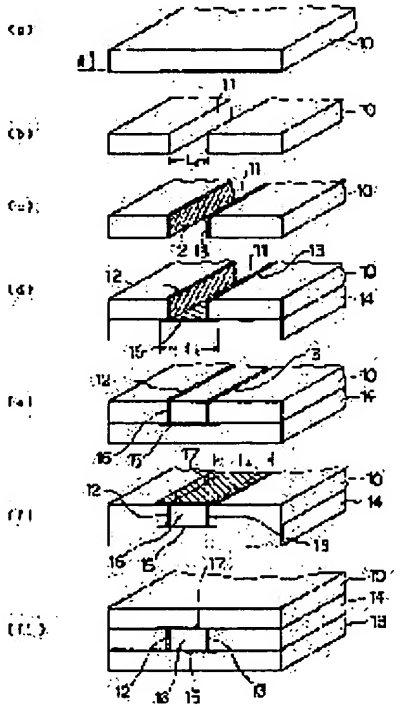
(22)Date of filing : 25.09.1997

(71)Applicant : KYOCERA CORP
(72)Inventor : TAKENOSHITA TAKESHI
UCHIMURA HIROSHI
FUJII MIKIO

(54) MULTILAYERED WIRING BOARD FOR HIGH-FREQUENCY AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a high-frequency multilayered wiring board provided with a transmission path composed of a dielectric wave guide in which a dielectric is encompassed by a conductor layer, and its manufacturing method.
SOLUTION: A slit 11 of width L1 is formed into a first insulating layer 10 composed of a dielectric and sidewall conductor layers 12, 13 are formed in a sidewall in the slit 11. Next, a first conductor layer 15 of a width L2 which is wider than a width L1 is formed at a position where the slit 11 is totally closed on an upper face of a second insulating layer 14 composed of a dielectric and the second insulating layer 14 is laminated so as to close the slit 11 by a first conductor layer 15 on a lower face of the first insulating layer 10. The slip 11 is filled with a dielectric 16, and a second conductor layer 17 composed of a width L3 wider than a width L1 is formed on an exposed face of the dielectric 16 in the slit, to thereby produce a high-frequency multilayered wiring board provided with a dielectric wave guide comprising the first conductor layer 15, the sidewall conductor layers 12, 13, the dielectric 16, and the conductor layer 17.



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